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APPLICATION FOR LETTERS PATENT

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Methods For Forming Wordlines, Transistor Gates, And Conductive Interconnects, And Wordline, Transistor Gate, And Conductive Interconnect Structures

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TECHNICAL FIELD

The invention pertains to a number of semiconductor structures and methods for forming such structures, including gate stack structures, conductive line structures, conductive interconnect structures, and programmable-read-only-memory devices.

BACKGROUND OF THE INVENTION

A continuous challenge in semiconductor processing is to improve conductivity and performance of stacked semiconductor structures. Among the stacked semiconductor structures commonly utilized are gate stacks, wordlines, programmable-read-only-memory devices such as EPROMs and EEPROMs, and conductive interconnects. Formation of some of these prior art stacked structures is described with reference to Figs. 1-4. Figs. 1-2 pertain to the formation of a wordline or gate stack structure, and Figs. 3-4 pertain to the formation of a programmable-read-only memory device.

Referring to Fig. 1, a semiconductor wafer fragment 10 is illustrated at a preliminary processing step of a prior art process for forming a wordline or gate stack. Wafer fragment 10 comprises a semiconductive material substrate 12, and field oxide regions 14 over substrate 12. A gate dielectric layer 16, generally comprising silicon dioxide, extends between field oxide regions 14. A polysilicon layer 18

and a polycide (silicide) layer 20 are formed over field oxide regions 14 and gate dielectric layer 16.

Polysilicon layer 18 typically comprises polysilicon uniformly doped with a conductivity enhancing dopant (illustrated by stippling within layer 18). Polycide layer 20 comprises a metal silicide, such as tungsten silicide, molybdenum silicide, titanium silicide or cobalt silicide. The formation of polycide layer 20 typically comprises depositing a metal over polysilicon layer 18 and reacting the metal with polysilicon layer 18 to form a metal-silicide. The reacting can comprise thermal processing of the metal layer and polysilicon layer at, for example, temperatures of from about 600°C to about 800°C.

Referring to Fig. 2, layers 16, 18 and 20 are patterned to form a conductive stack, and specifically to form a wordline 24. Source/drain regions 25 are provided proximate wordline 24. Conductive wordline 24 comprises a transistor gate electrically connecting source/drain regions 25. The final transistor structure can be either a p-channel transistor (PMOS), or an n-channel transistor (NMOS), and can be incorporated within a CMOS construction.

The speed of devices comprising wordlines and conductive gates generally increases with increasing conductivities of the wordlines and conductive gates. Accordingly, it would be desirable to improve the conductivity of wordlines and transistor gates. A method for improving the conductivity of a doped layer is to "activate" the dopant within the

layer. Although the chemistry of dopant activation is not well understood, activation is thought to occur as dopant is dispersed from grain boundaries in a polysilicon layer to bulk polysilicon away from the grain boundaries. Dopants are typically activated by thermal processing.

Alternative procedures similar to those of Figs. 1 and 2 can be used to form a conductive polysilicon interconnect. Such interconnects can comprise a line of polycide over a polysilicon. Accordingly, such interconnects are similar to wordline 24, but lack dielectric layer 16.

The speed of devices comprising conductive interconnects can increase with increasing conductivities of the conductive interconnects. Accordingly, it would be desirable to improve the conductivity of conductive interconnects.

Referring to Figs. 3-4, a prior art process for forming a programmable-read-only memory (PROM) device is illustrated. In the embodiment of Figs. 3-4, similar numbering to that of the embodiment of Figs. 1-2 is utilized, with differences indicated by the suffix "a", or by different numbers.

Referring to Fig. 3, a wafer fragment 10a is illustrated at a preliminary step during formation of a programmable-read-only memory device. Wafer fragment 10a comprises a semiconductive material 12a over which is formed field oxide regions 14a and gate dielectric layer 16a. A first polysilicon layer 18a is formed over regions 14a and dielectric layer 16a. A second dielectric layer 26 and a second

polysilicon layer 28 are formed over first polysilicon layer 18a, and a polycide layer 30 is formed over second dielectric layer 26.

Polysilicon layers 18a and 28 comprise uniformly doped polysilicon, typically comprising a dopant concentration of greater than 1×10^{19} ions/cm^3.

Referring to Fig. 4, layers 16a, 18a, 20a, 26, 28 and 30 are patterned to form the resulting PROM device 32. Within device 32, the patterned first polysilicon layer 18a is typically referred to as a floating gate. The patterned second polysilicon layer 28 and polycide layer 30 together comprise a conductive line 33.

The speed of circuits comprising PROM devices can increase with increasing conductivities of the conductive line and floating gate. Accordingly, it would be desirable to improve the conductivities of conductive lines and floating gates.

SUMMARY OF THE INVENTION

The invention encompasses stacked semiconductor devices including gate stacks, wordlines, PROMs, conductive interconnecting lines, and methods for forming such structures.

In one aspect, the invention includes a method of forming a conductive line. A silicide layer is formed against a polysilicon layer. A conductivity-enhancing impurity is provided within the silicide layer. The polysilicon layer and the silicide layer are formed into a conductive line shape.

In another aspect, the invention includes a programmable-read-only-memory device comprising a first dielectric layer over a substrate, a floating gate over the first dielectric layer, a second dielectric layer over the floating gate, a conductive line over the second dielectric layer, and a metal-silicide layer over the conductive line. The metal-silicide layer comprises a Group III dopant or a Group V dopant.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 illustrates a semiconductor wafer fragment at preliminary step of a prior art method for forming a wordline.

Fig. 2 illustrates the Fig. 1 wafer fragment at a prior art step subsequent to that of Fig. 1.

Fig. 3 illustrates a semiconductor wafer fragment at preliminary step of a prior art method for forming PROM device.

Fig. 4 illustrates the Fig. 3 wafer fragment at a prior art step subsequent to that of Fig. 3.

Fig. 5 illustrates a semiconductor wafer fragment at preliminary step of a first embodiment method of the present invention for forming a wordline.

Fig. 6 illustrates the Fig. 5 wafer fragment at a step subsequent to that of Fig. 5.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

A first embodiment of the present invention is described with reference to Figs. 5 and 6. In describing the first embodiment, like numerals from the preceding discussion of the prior art are utilized where appropriate, with differences being indicated by the suffix "b" or with different numerals.

Referring to Fig. 5, a semiconductor wafer fragment 10b is illustrated at a preliminary processing step. Wafer fragment 10b comprises a semiconductive material substrate 12b, such as, for example, monocrystalline silicon. Field isolation regions 14b and a gate dielectric layer 16b are formed over semiconductive material 12b. Field isolation regions 14b and gate dielectric layer 16b comprise an insulative material, such as, for example, silicon dioxide.

A conductive layer 18b and a polycide layer 20b are formed over field isolation regions 14b and gate dielectric layer 16b. Conductive layer 18b preferably comprises polysilicon doped to a concentration of greater than 1×10^{19} atoms/cm^3 with a conductivity enhancing dopant. Polycide layer 20b is against conductive layer 18b and comprises a metal silicide doped with conductivity enhancing dopant (the dopant being indicated by stippling). Preferably, polycide layer 20b is doped to a

concentration of greater than 1 x 10^{18} atom/cm^3 with the conductivity enhancing dopant.

Polycide layer 20b can comprise, for example, a metal selected from the group consisting of tungsten, tantalum, titanium, molybdenum and cobalt. Polycide layer 20b can be formed by the prior art method of depositing a metal over polysilicon layer 18b and reacting the metal with polysilicon layer 18b at temperatures of from about 600°C to about 800°C to form silicide layer 20b. Alternatively, and preferably, the thermal processing to form polycide layer 20b encompasses rapid thermal processing (RTP). In the context of this document, RTP refers to a process wherein a temperature is ramped at greater than about 7°C/second. Preferably, the RTP temperature is ramped to exceed 850°C and is maintained above 850°C for at least 10 seconds. Such RTP can activate dopant within polycide layer 20b to increase the conductivity of doped polycide layer 20b.

The RTP preferably occurs while exposing silicide layer 20b to an oxygen-comprising atmosphere, such as, for example, an atmosphere comprising at least one compound selected from the group consisting of O_2, O_3, N_2O and NO. Under such preferred conditions, a silicon dioxide layer 35 can be formed over polycide layer 20b. Silicon dioxide layer 35 can impede or prevent dopant diffusion outwardly from layer 20b and thereby advantageously retain dopant within layer 20b. It is noted that while the RTP preferably occurs while exposing layer 20b to an oxidizing

atmosphere, the RTP will generally also activate dopant within layer 20b if conducted while exposing layer 20b to a non-oxidizing atmosphere.

Wafer 10b differs from wafer 10 of the prior art (shown in Figs. 1 and 2) in that polycide layer 20b is doped with a conductivity-enhancing impurity, whereas the prior art polycide 20 (shown in Figs. 1 and 2) is not doped. As indicated above, the conductivity-enhancing dopant is preferably provided to a concentration of greater than 1 x 10^{18} atom/cm^3. Suitable conductivity enhancing dopants can comprise, for example, Group III or Group V dopants, such as dopants comprising boron, phosphorous or arsenic. Methods for doping silicide layer 20b include, for example, implanting dopant into the layer after formation/deposition of the layer, *in situ* doping of the layer during either chemical vapor deposition (CVD) or sputter deposition, and out-diffusion from a doped polysilicon layer 18b beneath silicide layer 20b.

An example CVD process for forming a polycide layer 20b comprising tungsten silicide doped with phosphorus (WSi_xP_y) comprises utilization of WF_6, SiH_4 and PH_3 as precursor materials in a CVD reactor. Alternatively, dichlorosilane can be substituted for SiH_4. Also, alternative dopant hydrides can be substituted for PH_3 to form a polycide doped with an alternative dopant. Such alternative metal hydrides can include, for example, AsH_3 or diborane. Also, other organic precursors comprising Group III or Group V dopants can utilized as alternative sources of dopant.

An example sputter deposition process comprises utilization of a target comprising a mixture of a source of metal, a source of silicon and a source of conductivity-enhancing impurity. The target is sputtered to form a silicide layer 20b comprising the conductivity-enhancing impurity and the metal.

Referring to Fig. 6, layers 16b, 18b, 20b, and 35 are patterned to form a conductive line 24b. Source/drain regions 25b are formed within substrate 12b such that conductive line 24b comprises a stacked transistor gate structure which electrically connects source/drain regions 25b. The resulting transistor structure can be a PMOS transistor or NMOS transistor, and can be incorporated into a CMOS structure.

Conductive line 24b differs from conductive line 24 (shown in Fig. 2) in that line 24b comprises a silicide layer 20b doped with conductivity-enhancing impurity. Such doping of layer 20b can lower the resistance of layer 20b relative to that of layer 20 (shown in Fig. 1) and thereby improve the performance of conductive line 24b relative to that of conductive line 24 (shown in Fig. 2). The above-discussed RTP can further improve the conductivity of layer 20b by activating dopant within layer 20b.

Although layer 20b is doped prior to patterning of layer 20b to form wordline 24b in the shown method, in alternative embodiments layer 20b can be doped after such patterning. As an example method of accomplishing such alternative embodiments, layer 20b could be doped by

ion implanting a conductivity enhancing dopant into layer 20b after patterning of layer 20b to form wordline 24b. As another example method, layer 20b can be doped by out-diffusion from conductively doped layer 18b by thermal treatment of wordline 24b.

The doped silicide of the present invention can be incorporated into numerous circuit device structures, including, for example, programmable-read-only-devices such as EPROMS and EEPROMS.

To aid in interpretation of the claims that follow, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.